UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,207	10/30/2003	Seok-Joon Park	SAM-0457	2219

7590 09/26/2007

Steven M. Mills
MILLS & ONELLO LLP
Suite 605
Eleven Beacon Street
Boston, MA 02108

EXAMINER	
SHAPIRO, LEONID	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
09/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/697,207	PARK ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4.7-12,14-16,18-20,22-23,25-26,28* is/are rejected.

7)☐ Claim(s) *5,6,13,17 and 21,24,29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-4, 7-8,14-16,22-23,25-28, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohmuro et al. (Pub. No.: US 2006/0017677 A1) in view of Maeda et al. (6,091,389).

As to claims 1,27 Ohmuro et al. teaches a response time accelerator for driving a liquid crystal display (LCD) (See paragraphs 0016-0018) comprising:

a frame memory unit that updates and stores one of previous data (See Fig. 9, item 53, paragraph 0085);

a table memory unit that stores predetermined mapped panel output values, predetermined mapped panel characteristic values, and flag information corresponding to the predetermined mapped panel characteristic values (See Fig. 9, items 55-56, paragraph 0086); and

an acceleration unit that reads the previous data corresponding to input current data and reads and decodes the predetermined mapped panel output value, predetermined mapped panel characteristic value, and flag information corresponding to the previous data and current data, performs interpolations on the decoded mapped panel output value and mapped panel characteristic value according to the flag

information, and generates liquid crystal panel data to be output to a liquid crystal panel (See Fig. 9, items 53-58, paragraphs 0084-0086) and previous data of a next frame (in the reference is equivalent to secondary frame memory) to be output to the frame memory unit (in the reference is equivalent to primary frame memory) (see in paragraph 0086: "alternately stored in the primary and secondary frame memories in each frame period...").

Ohmuro et al. does not explicitly disclose flag information corresponding to the previous data and current data, performs interpolations on the decoded mapped panel output value and mapped panel characteristic value according to the flag information.

Ohmuro et al. teaches a display status change pixel detection circuit for comparing data of primary frame memory with data of the secondary frame memory, and outputting the compensation voltage (See Fig. 9, items 53-58, paragraphs 0084-0086).

Since flag information is only one of software interpretations of the response time accelerator (in the reference correspondent to generation of the compensation voltage), it would have been obvious to one of ordinary skill in the art at the time of the invention to use flag information as software implementation of the generation of the compensation voltage to shorten the response time (See abstract in the Ohmuro et al. reference).

Omura et al. does not teach wherein the acceleration unit determines a gray level at which to generate the liquid crystal panel data based on the flag information set

in a previous frame, and wherein the flag information for a next frame is set based on a comparison of current data and the previous data of the next frame .

Maeda et al. teaches the flag information for a next frame is set based on a comparison of the current data and the previous data of a next frame is set based on a comparison of current data and the previous data of the next frame (fig. 9, col. 12, lines 5-26).

It would have been obvious to one of ordinary skill in the art at the time of the invention teachings of Maeda et al. into Omura et al. system in order to use flag for further processing (col. 12, lines 18-26 in the Maeda et al. reference).

As to claim 14, Ohmuro et al. teaches a method for improving a response time of a liquid crystal display (LCD) performed in a response time accelerator (See paragraphs 0016-0018) having a frame memory unit for updating and storing one or more frames of previous data (See Fig. 9, item 53, paragraph 0085), a table memory unit for storing predetermined mapped panel output values, predetermined mapped panel characteristic values, and flag information corresponding to the predetermined mapped panel characteristic values (See Fig. 9, items 55-56, paragraph 0086), the method comprising the steps of:

receiving current data in the acceleration unit;

reading the previous data corresponding to the current data in the acceleration unit;

reading and decoding the predetermined mapped panel output value, predetermined mapped panel characteristic value, and flag information corresponding

to the previous data and current data in the acceleration unit;

performing interpolation on the decoded predetermined mapped panel output value according to the flag information and generating liquid crystal panel data to be output to the liquid crystal panel in the acceleration unit; and

performing interpolation on the decoded predetermined mapped panel characteristic value according to the flag information and generating previous data of a next frame to be output to the frame memory unit in the acceleration unit (See Fig. 9, items 53-58, paragraphs 0084-0086) and previous data of a next frame (in the reference is equivalent to secondary frame memory) to be output to the frame memory unit (in the reference is equivalent to primary frame memory) (see in paragraph 0086: "alternately stored in the primary and secondary frame memories in each frame period...").

Ohmuro et al. does not explicitly disclose flag information corresponding to the previous data and current data, performs interpolations on the decoded mapped panel output value and mapped panel characteristic value according to the flag information.

Ohmuro et al. teaches a display status change pixel detection circuit for comparing data of primary frame memory with data of the secondary frame memory, and outputting the compensation voltage (See Fig. 9, items 53-58, paragraphs 0084-0086).

Since flag information is only one of software interpretations of the response time accelerator (in the reference correspondent to generation of the compensation voltage), it would have been obvious to one of ordinary skill in the art at the time of the invention to use flag information as software implementation of the generation of the

compensation voltage to shorten the response time (See abstract in the Ohmuro et al. reference).

Omura et al. does not teach wherein the acceleration unit determines a gray level at which to generate the liquid crystal panel data based on the flag information set in a previous frame, and wherein the flag information for a next frame is set based on a comparison of current data and the previous data of the next frame .

Maeda et al. teaches the flag information for a next frame is set based on a comparison of the current data and the previous data of a next frame is set based on a comparison of current data and the previous data of the next frame (fig. 9, col. 12, lines 5-26).

It would have been obvious to one of ordinary skill in the art at the time of the invention teachings of Maeda et al. into Omura et al. system in order to use flag for further processing (col. 12, lines 18-26 in the Maeda et al. reference).

As to claim 2, Ohmuro et al. teaches a comparator (in the reference pixel detection circuit) that compares the current data with the previous data and outputs the liquid crystal panel data and the previous data of the next frame with the same value as the current data, or the current data and the previous data (See Fig. 9, item 55, paragraph 0085);

a coefficient generator that generates coefficients to be used for interpolation based on the current data and previous data (See Fig. 9, item 56, paragraph 0085);

a table decoder that reads and decodes the predetermined mapped panel output value, predetermined mapped panel characteristic value, and flag information

corresponding to the previous data and current data (See Fig. 9, items 55-56, paragraphs 0084-0086);

a panel output interpolator that performs interpolation on the decoded predetermined mapped panel output value and generates the liquid crystal panel data (See Fig. 9, item 57, paragraphs 0082-0086);

a frame memory output interpolator that performs interpolation on the decoded predetermined panel characteristic value and generates the previous data of the next frame (See Fig. 9, items 55-57, paragraphs 0082-0086);

a panel output selector that selectively receives the output of the comparator or the output of the panel output interpolator and outputs the liquid crystal panel data (See Fig. 19, item 208, paragraph 0117); and

a frame memory output selector that selectively receives the output of the comparator or output of the frame memory output interpolator and outputs the previous data of the next frame (See Fig. 19, item 208, paragraph 0117).

As to claims 3-4,7-8,15-16,25 Ohmuro et al. does not explicitly disclose flag information corresponding to the previous data and current data, performs interpolations on the decoded mapped panel output value and mapped panel characteristic value according to the flag information.

Ohmuro et al. teaches a display status change pixel detection circuit for comparing data of primary frame memory with data of the secondary frame memory, and outputting the compensation voltage (See Fig. 9, items 53-58, paragraphs 0084-0086).

Since flag information is only one of software interpretations of the response time accelerator (in the reference correspondent to generation of the compensation voltage), it would have been obvious to one of ordinary skill in the art at the time of the invention to use flag information as software implementation of the generation of the compensation voltage to shorten the response time (See abstract in the Ohmuro et al. reference).

As to claims 22,26,28 Maeda et al. teaches determination based on the flag information set in the previous frame whether or not to generate the liquid crystal panel data at a maximum level or a minimum level (fig. 9, col. 12, lines 5-26).

2. Claim 9-12, 18-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Ohmura et al. as applied to claims 1,14 above, and further in view of Younis et al. (US Patent No. 6,292,122 B1).

Ohmuro does not teach the predetermined mapped panel output values and the predetermined mapped panel characteristic values correspond one-to-one to gray level values determined by MSB bits of the current data and previous data.

Younis et al. teaches the predetermined mapped panel output values and the predetermined mapped panel characteristic values correspond one-to-one to gray level values determined by MSB bits of the current data and previous data (See Fig. 6, items MSB,616, col. 10, Lines 21-35).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teachings of Younis et al. into Ohmuro et al. system in order to provide the faster response time (See Col. 2, Lines 7-9 in the Younis et al. reference).

Allowable Subject Matter

3. Claims 5-6,13,17,21,24,29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claims 5-6, 17 the major difference between the teaching of the prior art of record (Ohmuro et al. and Maeda et al.) and the instant invention is that the interpolation is performed using the following equation:

I=Pn-1 (DB-I :DB-n)

m=Pn(DB-1 :DB-n)

r=Pn-1IDB-(n+1):0)

s=Pn(DB-(n+1):0)

A={TP(I,m) **$(2_{(DB-n)}$ -r) +Tp(I+1,m)***r}>(DB-n)

C={TP(I,m+1) $(2_{(DB-n)}$ -r) +TP (I+1,m)*r}>(DB-N)

PZ={A* $(2_{(DB-n)}$-s) +C*s}>(DB-n)

where Pn, Pn-I , and TP denote the current data, previous data, and a mapped panel output value or a mapped panel characteristic value, respectively, and DB, n, and PZ are the number of data bits, the number of bits after truncation, and an output value, respectively.

Relative to claims 13,21 the major difference between the teaching of the prior art of record (Ohmuro et al. and Maeda et al.) and the instant invention is that the comparison is performed using the following equation:

I(Pn - 1) - (PN)I <= THV --> PO = Pn,pPn = Pn

where Pn-I, Pn, and THV denote the previous data, the current data, and a predetermined threshold value, respectively, and PO and pPn are the liquid crystal panel data and previous data of the next frame.

Relative to claims 24,29 the major difference between the teaching of the prior art of record (Ohmuro et al. and Maeda et al.) and the instant invention is that the acceleration unit generates the liquid crystal panel data which is the same as the current data and generates the previous data of the next frame which is the same as the current data, if the difference between the previous data and the current data is within a predetermined range.

Response to Arguments

4. Applicant's arguments with respect to claims 1-4.7-12,14-16,18-20 have been considered but are moot in view of the new ground(s) of rejection.

Telephone Inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LS
09.23.07

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600